Fractal Logic on Natural Substrates: From Engineerable Cellular Automata to Hybrid Self-Assembly and Dark-Sector Thought Experiments

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What would it take to build a trillion-transistor-class, *usefully programmable* computing unit without starting from CMOS? This paper develops a concrete, engineering-first pathway that begins with cellular automata (CA) redesigned as a hardware substrate (wires, clocks, fan-out, error states), scales via fractal floorplans (H-tree clocks, quadtree placement, Hilbert backbones), and meets matter through hybrid manufacturing that marries lithographic anchors to bottom-up, rule-driven self-assembly. We then widen the lens: if nature offers ultra-low-coupling media—up to and including speculative dark-sector fields—what could we learn about *field-native* information processing? Even if dark matter is not intelligent, treating it as a substrate clarifies minimum requirements for statefulness, communication, energy flow, and error control; it also yields lab programs (BECs, nonlinear optics) and sky-facing tests (algorithmic structure in pulsar timing, lensing, and stellar streams). The through-line is practical: specify rules that restore signals, enforce discipline, and compile from HDL; organize layouts fractally for clocking, routing, and repair; use top-down scaffolds to register bottom-up growth; and apply conservative governance ("do no irreversible harm") when hypotheses touch cosmic structure. The result is a unified research agenda for logic on grids, in materials, and—cautiously—in fields.

Keywords: cellular automata engineering, dual-rail logic, GALS clocking, fractal floorplanning, H-tree, Hilbert backbone, quadtree placement, trillion-transistor equivalent, directed self-assembly, hybrid lithography, error-correcting tiles, field-native computing, axion-like fields, gravitational SETI, algorithmic structure search, embodied mesh, governance and ethics.

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1. Motivation and Scope

1.1 Why leave CMOS: scaling walls, cost, and new media

CMOS has delivered exponential improvements for half a century, but three converging walls now make “more of the same” a poor bet for new compute frontiers:

- **Physics limits.** Transistor gate lengths and interconnect pitches are in regimes where variability, leakage, and parasitics dominate. Power density caps clock frequency; wire delay and RC stacks—not device speed—limit system performance. Variability at atomic scales turns deterministic designs into statistical ones.
- **Cost curves.** Leading-edge fabs, masks, and EUV/High-NA toolchains push nonrecurring engineering into the billions. Only a handful of products justify the fixed costs. Innovation becomes permissioned, not exploratory.
- **System bottlenecks.** Memory walls, I/O locality, and energy per bit moved now dwarf energy per operation. Even perfect transistors can’t beat slow, hot, long wires.
- **Opportunity cost.** Alternative substrates (programmable materials, programmable fields, self-assembling lattices) promise different trade spaces: volumetric density, self-healing redundancy, in-situ sensing/actuation, and closer coupling to the physical environment.
- **Design latitude.** Outside CMOS we can re-choose primitives—signals as tokens not voltages, field phases not logic levels, redundancy and error detection as first-class citizens—matching computation to the medium rather than coercing the medium into a CMOS look-alike.

Leaving CMOS isn’t a rejection of silicon; it’s a diversification strategy: keep lithography where it’s unrivaled (registration, vias, global interconnect), and explore new substrates where it’s weak (3-D repetition, low-dissipation field dynamics, hierarchical self-repair).

1.2 Design criteria: engineerability, routability, fault tolerance, compilability

Any non-CMOS path that aspires to “trillion-transistor-equivalent” usefulness must satisfy four criteria simultaneously:

- **Engineerability (local rules with global guarantees).**
  The substrate must support a small, orthogonal **cell/gate library** with predictable timing and signal restoration. In CA terms: dual-rail tokens, repeaters, legal/illegal interaction masks, and a sticky error state. In materials: binding rules with large energy gaps between allowed and forbidden joins. In fields: stable excitations (solitons/vortices) with controllable interactions.

- **Routability (scalable communication).**
  Computation fails without communication. We need crossings, fan-out, and long-distance channels that do not avalanche errors. Practically, this implies **hierarchical networks**: regular local grids for short hops and **fractal backbones** (H-trees/Hilbert paths) for global moves. Vias or "overpasses" must exist in whichever form the medium allows.

- **Fault tolerance (detect, contain, recover).**
  Non-CMOS media will be defect-rich. Bake in **error signaling**, **isolation boundaries**, and **redundancy** (e.g., TMR tiles, N-of-M sparing, periodic scrub-and-heal). Faults should localize, not cascade; healthy regions must continue operating during repair or reconfiguration.

- **Compilability (from high-level intent to layout/run).**
  Value comes from a **toolchain**: map HDL or dataflow graphs to substrate macrocells, place within bounded-latency tiles, route with guaranteed capacity, insert synchronizers where domains meet, and produce artifacts you can simulate and then fabricate or grow. Without an automated compile path, demonstrations will remain artisanal and unscalable.

These criteria are medium-agnostic. They form the yardstick by which we judge grids (cellular automata), matter (hybrid self-assembly), and fields (dark-sector analogs).

1.3 Three arenas: grids (CA), matter (hybrid self-assembly), fields (dark-sector hypothesis)

We pursue the same architectural ideas across three physical regimes to maximize transfer of insight:

- **Grids (Cellular Automata).**
  What it is: A uniformly updated lattice whose **local rules** are chosen to emulate digital discipline: wires, gates, latches, routers, clocks.
  Why here: CA give controllable experiments in large-scale layout, timing, congestion, and error dynamics without materials risk. They let us **prove engineerability** (clean signal restoration, legal/illegal interaction masks), develop **fractal floorplans** (H-tree clocks, quadtree fault containment), and validate **compilers** (HDL → macrocell stamps → routable leaf tiles).
  Deliverable: A working "trillion-equivalent" blueprint built from many synchronized CA tiles with hierarchical networks and live fault isolation—demonstrating the criteria end-to-end in silico.

- **Matter (Hybrid Self-Assembly).**
  What it is: A **hybrid** process where lithography lays down **anchors**—fiducials,

power/clock rails, I/O vias—while **rule-driven tiles** (DNA origami, block copolymers, patchy nanoparticles) **self-multiply** into dense, regular fabrics.
Why here: Lithography excels at registration and metal; **rules excel at repetition and 3-D**. The hybrid approach aligns with our criteria: engineerable binding libraries (allowed/forbidden motifs), routable channels via templated trenches/backbones, fault tolerance via kinetic proofreading and majority tiles, and compilability via stampable macrocells (crossbars, CAMs, FIFO grids) that a placer/router can target.
Deliverable: First-generation arrays (memory-like or photonic/phononic) with measured yield, built-in scrubbing, and litho-connected buses—moving beyond "beautiful crystals" to **programmable, repairable** fabrics.

- **Fields (Dark-sector hypothesis and lab analogs).**
  What it is: Treat coherent fields (ultralight bosons, self-interacting media, dark photons) as **computational substrates** whose excitations act as logic primitives. Use **laboratory analogs** (BECs, nonlinear optics) to prototype "field-native computing."
  Why here: Fields push us toward **ultra-low-dissipation, reversible** information processing and **long-horizon stability**—properties desirable even on Earth. Even if cosmic dark matter is not intelligent, modeling **how one would write, move, and protect information** in weakly coupled media refines our error models and energy accounting.
  Deliverable: Lab-validated **write/erase protocols** (parametric pumping, phase codes), stability maps for topological memories, and **observational tests** (algorithmic-structure searches in pulsar timing, lensing, stellar streams) that either constrain or inspire new mechanisms—feeding back into CA/matter designs.

Scope. The paper develops a single, cross-arena design language—signals as tokens, hierarchical clocks, boundary contracts, redundancy, and compilers—that readers can apply on grids, in materials, and (cautiously) in fields. The aim is not to replace CMOS everywhere but to **open high-value niches** where new media deliver density, efficiency, resilience, or embodiment that silicon alone cannot.

2. An Engineerable Cellular Automaton for Logic

2.1 Rule class: partitioned/block CA with radius-2 neighborhoods

Why partitioned? A block (Margolus) CA composes the global update from local **permutations**, avoiding rule conflicts and race conditions. We alternate checkerboard tilings so signals move and interact predictably.

Concrete choice

- **Lattice:** 2-D square grid.
- **Partitioning:** 2×2 Margolus blocks; alternate offset each tick.
- **Interaction horizon:** Effective **radius 2** via a two-stage pipeline per tick:
    1. **Transport pass** (permutation on each 2×2) moves/rotates tokens 1 cell.
    2. **Logic pass** (permutation on each 2×2) applies gate/fan-out/merge rules.
- **Priority stratification:** Within each pass, sub-permutations execute in a fixed order: clock → transport → gate/collision → sanitation (absorb/clip) → error propagation.

Engineering invariants

- (I1) At most one **signal token** per rail per cell after a pass.
- (I2) Permutations are **bijective** on the set of legal local patterns (no spontaneous token creation).
- (I3) Any illegal pattern maps to **E (error)** deterministically.

2.2 State budget and cell library: wires, corners, vias, split/merge, repeaters, error

We allocate ~16–20 states to keep the rule table compact but expressive.

Core states (suggested S = 18)

- **.** Empty / void
- **I** Insulator / shield
- **C** Conductor (straight segment)
- **K⊥, K⊣** Corner variants (two orientations)
- **A, B** Dual-rail signal tokens (logic 0 and 1 carriers)
- **R** Repeater / regenerator
- **F** Splitter (legal 1→2 fan-out site)
- **M** Merger (legal 2→1 fan-in site for dual-rail)
- **V↑, V↓** Via pair (enter/exit “overpass” layer)
- **A^+, B^+** Overpass-layer tokens (non-interacting with plane except at V)

- **T0, T1, T2, T3** Clock phase tiles (see §2.4)
- **E** Error (sticky, slow-spreading alert)

Corners (K), repeaters (R), split/merge (F/M), and vias (V) are **geometry-encoded**: the surrounding conductor/insulator layout disambiguates orientation, so we don't need separate state symbols for all rotations.

Local legality masks

- Signals **A/B** may only occupy **C/K/R/F/M/V** cells in the direction permitted by the mask; touching **I** without a legal port maps to absorption (A/B → .) during sanitation.
- Overpass tokens **A^+/B^+** only interact with **V** and **I**; they pass "over" **C/K** without coupling.

2.3 Signal discipline: dual-rail tokens, automatic regeneration, sticky error state (E)

Dual-rail encoding

- Logical value carried by **presence** of a one-cell pulse:
  – **0:** token **A** on rail-0; rail-1 empty
  – **1:** token **B** on rail-1; rail-0 empty
  – **Illegal:** both rails active or both empty at a sample point → **E**
- Advantages: no DC levels, easy **error detection**, robust against pulse drift.

Transport

- In the **transport pass**, a token advances one cell along its rail if the next cell is free and legal. At a **corner K**, transport rotates heading; at **V↑/V↓**, tokens switch planes A⇄A^+ (B analogously).

Automatic regeneration

- Passing through **R** transforms any 1–2-cell smear back to a **canonical one-cell pulse** and resets its **age tag** (implicit in the permutation schedule). Place **R** every *d* cells (design parameter; e.g., every 8–12 hops).

Gate semantics (collision computing with discipline)

- **Gate footprints** are small motifs (e.g., 2×3, 3×3) where two rails cross with geometry that only allows specific meetings on **Tϕ** (clock phase). The **logic pass** maps input token pair(s) to output token(s) per truth table.

    - Example: NAND—if tokens arrive concurrently on both inputs at ϕ=1, emit **A** on output rail at ϕ=2; all other legal arrivals emit **B** appropriately (library defines exact mappings).

- **Fan-out (F):** Duplicate one input token into two outputs **iff** both target cells are clear; else set **E** on the junction to flag contention.
- **Merge (M):** For dual-rail, **OR** merge is legal if ≤1 token present per rail across inputs; illegal overlaps → **E**.

Error behavior (sticky)

- **Generation:** Any illegal pattern (e.g., simultaneous drivers, token hitting shield, empty sample when a rail asserts "must carry") maps to **E**.
- **Propagation:** E persists in place for k ticks, then **creeps** one cell along designated **alert channels** (thin wires) so monitors can localize.
- **Quarantine:** Neighbor transport rules treat **E** as **opaque**; tokens do not traverse through E until a supervisor (watchdog macrocell) scrubs or remaps.

2.4 Timing: tiled 4-phase clocks and GALS handshakes

Local 4-phase clock

- Clock is carried by **T0–T3** tiles arranged in a **static pattern** (e.g., 2×2 periodic tiling). Each tick advances **Tϕ → Tϕ+1 mod 4**.
- **Semantic contract** (example):
    - **ϕ0: sample** latch inputs; **F/M** eligibility check.
    - **ϕ1: transport** step for tokens (move one cell).
    - **ϕ2: collision/gate** evaluation; generate outputs.
    - **ϕ3: regeneration/sanitation** (R pass, absorbs strays); prepare next sample.

This yields **deterministic 2-cycle gate latency** (transport+logic), with regeneration before the next sample.

Global-asynchronous/local-synchronous (GALS)

- The grid is partitioned into **leaf tiles** (e.g., 64×64) each covered by a **phase-consistent clock patch** (identical T-tiling).

- Adjacent tiles may run with slight **phase offsets** or **divided clocks** (e.g., parent tile at 1/2 rate). Cross-tile links include a **ready/valid shim** implemented in states:
    - **VALID** rail (A_V/B_V tokens) announces data present.
    - **READY** rail acknowledges consumption.
    - Transfer completes only when VALID∧READY observed at **ϕ0**; otherwise sender holds (no data loss) and downstream back-pressure propagates.

Clock distribution (layout)

- Use an **H-tree** pattern of T-tiles to keep skew bounded in large layouts; regenerate T via small **clock repeaters** (local permutations that re-phase T tiles).

2.5 Memory and flow: latches, FIFOs, back-pressure

Latches (L) and registers

- **L-macrocell** footprint (e.g., 3×3 or 4×4):
    - On **ϕ0**, if **WRITE-ENABLE** rail carries a token, **sample** the dual-rail data inputs; store as an internal latent token pair (encoded in a tiny loop).
    - On **ϕ2**, **present** stored value to output rails (A/B token emission).
- **DFF** = two L cells in master–slave arrangement offset by one phase to prevent transparency.
- **Register file**: 2-D array of L cells; select lines are dual-rail, decoded locally by splitters/mergers; periodic **R** elements ensure stable readout.

FIFOs and flow control

- **FIFO stage** = {L cell + handshake shim}:
    - **Enqueue** when upstream asserts VALID and the stage asserts READY.
    - **Dequeue** when downstream asserts READY and the stage holds VALID.
- Chain k stages for depth-k FIFO; latency per hop is 2–3 ϕ steps; throughput = one token per ϕ cycle at saturation.
- **Elasticity:** Because handshakes are explicit rails, **back-pressure** propagates upstream automatically—no token loss, no global timing assumptions needed.

Branches and joins with flow

- **Split with flow:** F node emits **VALID** on both branches only when both downstream **READY** are present; otherwise it stalls, preventing partial duplication.
- **Join with flow:** M node asserts **READY** upstream only when the merged consumer is READY and the dual-rail legality holds.

Persistence and scrub

- Long storage lines include periodic **R** to reset pulse shape and optional **parity tiles** (simple duplication check) every *n* cells.
- **Watchdog macrocells** listen on **E-alert** channels; upon detection, they:
    1. **Freeze** local ingress (de-assert READY),
    2. **Drain** or **flush** local buffers to a sink,
    3. **Scrub** (force sanitation permutations over a window),
    4. **Re-admit** traffic and raise a **health token** for supervisory logic.

Developer notes (for the toolchain)

- **Latency contracts:** Library entries declare **(L_in, L_out)** in ϕ steps; router sums wire costs as **1 per hop** plus **R** penalties; the compiler enforces **≤ budget** per net.
- **Placement constraints:** Macrocells expose **N/E/S/W** ports on fixed offsets; routers reserve dedicated **signal tracks** and separate **alert tracks** to avoid deadlocks.
- **Simulation harness:** Two-pass Margolus engine with rule tables keyed by (local 2×2 pattern, phase ϕ). Include invariant checks (I1–I3) and automatic **waveform probes** for VALID/READY rails to debug GALS crossings.

This CA design gives you **digital-logic discipline** (clean wires, gates, memory, timing) with **layout-native** supports for scaling (vias, crossings), **robust flow control** (explicit handshakes), and **safety hooks** (E state, watchguards)—the essentials you need before chasing fractal floorplans and trillion-equivalent assemblies.

3. Fractal Floorplans that Scale

3.1 H-tree clocks for low skew; quadtree fault containment

H-tree clocking. Lay a recursive H-tree over the CA fabric so each branch has equal path length from root to leaf. At recursion depth d, each segment length halves; clock repeaters (tiny CA macrocells) sit at H joints to re-phase T0..T3. Because every leaf shares the same hop count from the root, phase error stays bounded by a constant number of CA ticks regardless of area. Practical contracts:

- Max skew within a leaf: ≤ 1 phi step.
- Max interleaf phase delta within a quadrant: ≤ 2 phi steps.
- Repeater spacing: every s cells (empirically s ≈ 16–32) to restore T tiles and clear clock "smear."

Quadtree containment. Partition the plane recursively into quadrants Q[d,i], where d is depth and i indexes siblings. Each node owns:

- a health channel (E-alerts bubbling up),
- ingress/egress FIFOs to siblings/parent,
- a local power/clock gate.
  On persistent error at leaf level, the parent Q[d] throttles only the affected child, reroutes flows via siblings, and optionally cold-swaps in a spare (3.4). Containment is guaranteed because traffic must traverse boundary routers that enforce legality and handshakes.

Operational modes per node

- RUN: normal timing; admit traffic.
- DRAIN: stop ingress; flush egress to parent sink.
- SCRUB: run sanitation permutations over a window; inhibit local clocks except T regenerators.
- ISOLATE: cut leaf; remap addresses; raise incident token upward.

3.2 Hilbert/Peano backbones for global communication

Why fractal backbones. Space-filling curves (Hilbert, Peano) preserve locality while visiting every leaf; adjacent addresses remain near in physical space, minimizing long congested links.

Backbone design.

- **Hilbert bus lanes:** 1–k parallel dual-rail lanes snake through leaves along a discrete Hilbert path. Each leaf exposes a small router macrocell with:
    - 2 local ports (N/S or E/W depending on traversal),
    - 1 local injection/ejection port,
    - virtual channels: {cmd, data, error}.
- **Addressing:** Use Morton/Z-order codes for leaf IDs so (x,y) bit-interleaving matches quadtree levels. Routing is table-free: forward toward the first differing quadtree bit.
- **Latency contract:** per-hop pipeline = 2 phi (transport+gate). End-to-end latency L ≈ 2*H hops, where H is Manhattan hops along the curve segment between source and dest leaf entries.

Congestion control.

- Credit-based: each router advertises free slots; injection throttled without credits.
- Age priority: older flits win ties to prevent livelock.
- Detours: optional local grid bypass between near neighbors inside the same parent Q[d] to avoid backbone for short exchanges.

Broadcast/collect.

- Top-down broadcast leverages H-tree (clock/reset/config tokens) with guaranteed time windows.
- Bottom-up reduce (sum, popcount, min/max) accumulates along quadtree edges; leaves emit partials, parents combine.

3.3 Leaf-tile microgrids and boundary contracts (latency, ready/valid)

Leaf definition. A leaf tile is an r×r CA microgrid (e.g., 64×64) containing only regular channels and standardized ports. Inside: Manhattan signal tracks, periodic repeaters R, latch islands L, and small crossbars for local fan-out.

Boundary ports.

- **Data ports:** dual-rail A/B with VALID/READY side rails.
- **Clock port:** T0..T3 tile continuity checks (leaf must align within ≤ 1 phi).
- **Alert port:** slow E-alert rail to parent.

- **Health port:** heartbeats and counters (dropped flits, retries, scrub cycles).

Contracts (checked by the compiler and runtime monitors).

- **Latency budget:** Each exported net declares a max latency L_max in phi steps across leaf + interleaf path; router must meet L_path ≤ L_max or reject placement.
- **Throughput budget:** Sustained injection ≤ lane capacity C (tokens per phi); compiler inserts rate limiters when needed.
- **Legality:** All boundary crossings must be guarded by GALS shims: VALID high without READY must stall; READY high with no VALID must be ignored; illegal dual-rail combinations at sampling map to E and are contained within a 1-leaf radius.

Verification hooks.

- On-leaf probes that mirror VALID/READY toggles to a local counter.
- Watchdog tiles that compare observed latency against L_max; violations raise a soft fault before E.

3.4 Redundancy: TMR leaves, N-of-M sparing, periodic scrubbing

TMR at the leaf level.

- Triplicate critical logic across three sibling leaves {L0,L1,L2} in the same parent Q[d].
- Majority-vote macrocell at parent boundary merges outputs per bit and emits E if no majority.
- Voters are pipelined to keep timing: vote latency <= 2–3 phi.
- Input distribution uses splitters with handshake so all three replicas see identical traffic; any divergence raises a health warning.

N-of-M sparing.

- For each quadtree parent, provision M leaves with N active at a time (e.g., N=3, M=4). A spare S remains cold or runs at low duty to keep T tiles fresh.
- On persistent E (k consecutive incidents or watchdog score > threshold), parent executes:
    1. DRAIN faulty leaf,
    2. ISOLATE and readdress routes to S (Morton code remap),
    3. LOAD state from neighbor snapshot FIFO if stateful, else reinit,

4. RUN and mark S as active; schedule faulty leaf for offline SCRUB+BIST.

Periodic scrubbing.

- **Clocked scrub tokens** traverse all rails every q cycles, forcing interaction with R and sanitation rules:
    - Re-canonicalize pulses,
    - Clear orphan tokens,
    - Verify parity/checksum tiles.
- **Staggered schedule:** avoid global pauses by phase-offset scrubs per quadrant.
- **Telemetry:** leaves emit scrub counts, corrected errors, and time-since-last-E; supervisors adapt q (scrub periodicity) to error rate.

Degrade-gracefully policy.

- If multiple leaves fail beyond spare capacity, the fabric reduces service area:
    - Repartition workload to healthy quadrants,
    - Lower injection rates on backbone to preserve latency SLOs,
    - Advertise a reduced capability vector to the runtime (width, depth, bandwidth).

Summary. H-tree clocks bound skew, the quadtree localizes failure and manages power, Hilbert/Peano backbones deliver scalable global communication with locality, leaf-tile contracts make placement/routing predictable, and layered redundancy (TMR, sparing, scrub) converts frequent small faults into bounded, repairable incidents—enabling wafer-scale, trillion-equivalent CA systems to operate as dependable computers rather than physics toys.

4. From Gates to “Trillion-Transistor Equivalent”

4.1 Macrocell library (INV, NAND2, XOR, DFF, C-element, FIFO)

We standardize a small set of **stampable macrocells** that obey the CA timing and legality rules and expose fixed N/E/S/W ports.

- **INV (inverter / dual-rail swap).**
  Footprint: 6×6–8×8 cells. Latency: 1–2 phi. Ports: 1 in, 1 out. Internals: cross-coupled collision site + one R stage. Use: level restoration, clock buffering, polarity changes.

- **NAND2.**
  Footprint: 8×8–10×10. Latency: 2 phi (transport+gate). Ports: 2 in, 1 out. Internals: perpendicular rails with gated collision window on ϕ2, followed by R. Library provides mirrored variants for routing convenience.

- **XOR2.**
  Footprint: 10×10–12×12. Latency: 3 phi (two staged collisions). Ports: 2 in, 1 out. Internals: two controlled merges and one fan-out return path; uses an extra R to maintain pulse integrity.

- **DFF (edge-sampled flip-flop).**
  Footprint: 10×10–12×12. Latency: 2 phi (M-S latch pair across ϕ0/ϕ2). Ports: D, Q, optional EN. Internals: two L tiles, internal ready/valid shim, local T-tile checker.

- **C-element (Muller).**
  Footprint: 10×10–12×12. Latency: 2–3 phi. Ports: 2 in, 1 out. Internals: state-holding loop, outputs a token iff both inputs agree; emits E on illegal dual-rail overlap. Use: asynchronous joins, hazard filters, handshakes.

- **FIFO stage.**
  Footprint: 12×12–14×14. Latency: 2–3 phi per stage. Ports: data in/out with VALID/READY rails. Internals: L tile + handshake logic + R. Depth-k FIFO = k stamps in series.

- **Splitters/mergers (F/M).**
  Footprint: 6×6–8×8. Latency: 1–2 phi. Discipline: duplicate only when both targets READY; merge only if ≤1 token per rail; else raise E.

- **Router microcell (leaf edge).**
  Footprint: 12×12–16×16. Latency: 2 phi per hop. Ports: two backbone directions + one local injection/ejection. Internals: small flit buffer (2–4), virtual lanes {cmd,data,error}, credit counters.

All macrocells present **canonical ports** on fixed offsets so the placer can treat them as LEGO blocks; internal Rs are placed to guarantee pulse normalization at outputs.

4.2 Cost model: cells per macrocell, repeater spacing, wiring overhead

We define a simple parametric model to guide architecture-level sizing.

- **Cell area proxy.**
  Let A_gate be the average cell footprint:
  - INV ≈ 60 cells

- NAND2 ≈ 80 cells
- XOR2 ≈ 110 cells
- DFF ≈ 120 cells
- C-element ≈ 110 cells
- FIFO stage ≈ 150 cells
  These include intra-macro wiring, insulators, and mandatory repeaters.

- **Repeater spacing (R).**
  Place an R every s steps along a rail. s balances dispersion vs overhead.
  Typical $s \in [8, 12]$.
  Wire cost factor for a net with length L (in cell steps):
  $cells_wire(L) \approx L + \lceil L/s \rceil \cdot c_R$ where $c_R \approx 4–6$ (footprint of R motif).

- **Crossings and vias.**
  Each legal crossing consumes a **V** up/down pair and 2–3 sanitation cells: $c_V \approx 6–8$.
  Overpass tokens A+ / B+ incur no extra collisions, but you still pay the via footprint.

- **Wiring overhead factor (WOF).**
  For random-placement logic at density ρ (fraction of leaf usable for macrocells), empirical routing overhead scales superlinearly:
  $WOF(\rho) \approx 1 + \alpha \cdot \rho/(1-\rho)$, with $\alpha \approx 0.3–0.5$ for Manhattan channels.
  To keep WOF < 2, target $\rho \leq 0.6$; reserve ≥40% of leaf for tracks, Rs, and shims.

- **Latency budget.**
  Gate latency L_gate in phi: INV=1–2, NAND2=2, XOR2=3, DFF write/read=2 each.
  Wire latency $L_wire \approx \lceil L/s \rceil$ (one phi per R segment) + local turns.
  Path latency $L_path = \Sigma\, L_gate + L_wire + hops_backbone \cdot 2$.

- **“Transistor-equivalent” mapping.**
  Treat NAND2 as 4 transistors CMOS-equivalent. For a target **T_tran** transistors, required NAND count $N_NAND \approx T_tran/4$.
  With avg CA cost **$\bar{A}_NAND \approx 80$ cells**, raw logic cell budget $\approx 80 \cdot N_NAND$.
  Include overheads: total cells ≈ (logic cells + wire cells)·WOF + router+FIFO cells.

Worked scale example.
$T_tran = 10^{12} \Rightarrow N_NAND \approx 2.5\times10^{11}$.
Raw logic cells $\approx 80 \cdot 2.5\times10^{11} \approx 2.0\times10^{13}$.
Assume wiring adds ~40% before WOF: 2.8×10^{13}.

At $\rho \approx 0.55 \Rightarrow$ WOF $\approx 1.37 \Rightarrow \approx 3.8\times10^{13}$ cells.
This dictates partitioning into many leaves and chiplets (next section).

4.3 Tiling and chiplets: partition, paging, and energy-proportional ticking

Leaf and quadrant hierarchy.

- **Leaf tile:** r×r cells (e.g., 64×64 or 128×128) with fixed port locations.
- **Quadrant:** 2×2 leaves under one parent; recursion depth D yields 4^D leaves.

Chiplets on a wafer-scale CA.

- Define chiplets as **rectangular clusters of leaves** (e.g., 64×64 leaves) with internal high-rate clocks and boundary NoC links.
- Chiplets communicate via **Hilbert backbone** lanes with fixed bandwidth contracts.

Partitioning.

- Graph partitioner minimizes cut nets respecting quadtree boundaries; objectives:
    - fit leaf area (Σ macrocell areas + routing) ≤ $r^2 \cdot \rho_max$,
    - minimize interleaf nets (reduces router load),
    - co-locate latency-sensitive chains.

Paging (spatial & temporal).

- **Spatial paging:** inactive chiplets can be power-gated analogs: clocks slowed, tokens drained, T tiles maintained at low duty.
- **Temporal paging:** workloads with bursty demand are scheduled in **time slices**; leaf registers/FIFOs checkpoint state to neighbor buffers, enabling **hot-swap** for scrubbing.

Energy-proportional ticking.

- Tick rate f_leaf per leaf selected from {f_max, f/2, f/4, …}.
- Policy: set f_leaf ∝ queue depth + error-rate budget.
- Background **T-tile keepalive** runs at a minimal rate even when leaf is idle to preserve phase alignment.

Thermal distribution.

- Fractal clock + locality-preserving routing spreads hotspots. Scheduler avoids activating adjacent leaves at f_max if thermal telemetry crosses threshold; spill to spare leaves (N-of-M) when needed.

4.4 Toolchain sketch: HDL → placement/routing → CA bitmap

We require an **end-to-end compiler** that takes synthesizable HDL and emits a bit-accurate CA initial condition and rule set.

1. **Front-end synthesis.**
    - Parse Verilog/VHDL; tech-map to **CA macrocell library** (INV/NAND2/XOR2/DFF/C-element/FIFO).
    - Perform Boolean optimization and pipeline insertion to satisfy per-path L_max budgets; expose multi-cycle paths explicitly when needed.
2. **Leaf-aware partitioning.**
    - Hypergraph partitioner clusters macrocells into leaf bins with targets: area ≤ $r^2 \cdot \rho_max$, estimated wirelength minimized, timing slack ≥ 0.
    - Multi-objective: minimize interleaf net count and balance router bandwidth usage across Hilbert lanes.
3. **Placement.**
    - Inside each leaf, place macrocells on a **regular microgrid**; ports snap to channel tracks; keep-out regions for T tiles and alert rails.
    - Honor **port alignment** to boundary connectors; pre-reserve corner channels for backbone ingress/egress.
4. **Routing.**
    - **Intra-leaf:** Manhattan maze with costs: turn=+1, via V=+c_V, repeater every s steps inserted automatically.
    - **Inter-leaf:** Assign to (a) direct sibling link inside same parent, else (b) Hilbert backbone; compute hop count and allocate **virtual lanes** and **credits**.
    - Insert **GALS shims** at every boundary; attach VALID/READY rails; verify no combinational loops across leaves.

5. **Timing closure.**
    - Accumulate **phi-latency** along each path: sum gate and wire segments; ensure L_path ≤ L_max.
    - Where violated: add pipeline DFFs or re-partition; adjust leaf tick rates (if allowed) as a last resort.
6. **Reliability insertion.**
    - For designated critical paths/blocks: triplicate placement across sibling leaves; insert majority voters and consistent input splitters; route **E-alert** taps to parent monitors.
    - Place **scrub loops** and parity tiles at policy-defined intervals.
7. **Emission.**
    - Generate the **CA bitmap**: a tiled image of cell states (. I C K R F M V A B A+ B+ T0..T3 E) for each coordinate.
    - Generate the **rule table**: partitioned permutations for transport and logic passes keyed by local patterns and phase.
    - Output **manifest**: leaf tick rates, router lane allocations, latency/throughput budgets, scrub schedules.
8. **Verification & sim.**
    - Run cycle-accurate CA simulation with invariant checks (one token per rail per cell, no illegal crossings, GALS protocol compliance).
    - Fault-injection suite: random token drops, stuck-E cells, local clock skew; verify containment (quadtree) and recovery (scrub + sparing).
9. **Runtime control plane.**
    - Provide a minimal **supervisor** that can: throttle leaves, trigger DRAIN/SCRUB/ISOLATE, remap Morton addresses to spares, adjust f_leaf, and collect telemetry (latency histograms, E-counts, scrub stats).

Outcome. This toolchain makes the CA fabric **compilable** like an ASIC/FPGA: you write HDL, get a placed/routed CA image with timing/reliability guarantees, and run it at scale. With fractal floorplans and redundancy, the same flow scales from demo-class leaf arrays to **trillion-transistor-equivalent** assemblies.

5. Lithography vs Rule-Driven Molecular Placement

5.1 Strengths/limits of top-down patterning (overlay, defectivity, interconnect)

Strengths

- **Overlay & registration.** Top-down scanners deliver sub-nanometer overlay and deterministic layer-to-layer alignment. This underwrites dense vias, tight SRAM cells, and multi-layer logic with predictable timing.
- **Defectivity control.** Mature photo/etch/clean stacks achieve part-per-billion–class line defects over reticle fields via redundancy, in-line metrology, and statistical process control; parametric drift is monitored wafer-by-wafer.
- **Pattern versatility.** Arbitrary 2-D geometries (within design rules) across multiple layers; rule decks encode forbidden pitches, cut masks, coloring, etc., enabling complex standard-cell libraries.
- **Metals & vias.** Established BEOL: selective barriers, Cu/Co/Ru interconnect, air-gaps/ULK dielectrics, CMP planarity—critical for routability and low contact resistance.
- **Tooling & PDKs.** Industrial PDKs, timing corners, extraction flows, and sign-off criteria make large designs compilable and verifiable at scale.

Limits

- **Cost & scale granularity.** Masks/tooling push NRE into the billions; iteration cycles are slow, locking out exploratory architectures and bespoke designs.
- **3-D volumetric density.** True 3-D free-form structures are hard; stacking is mostly planar (FEOL/BEOL tiers, 3D-NAND, hybrid bonding) with thermal and alignment constraints.
- **Interconnect dominance.** RC delay, via resistance, and electromigration dominate at advanced nodes; wire energy per bit moved often exceeds compute energy.
- **Regularity penalty.** Extremely regular fabrics (crossbars, CAMs) incur the same capex as arbitrary logic; litho cannot “exploit repetition” to lower marginal patterning cost per instance.
- **Process windows.** Line-edge roughness, stochastic resist effects, and etch bias create variability that must be fought with restrictive design rules and redundancy.

5.2 Where rules win: repetition, 3-D structure, hierarchical redundancy

Strengths of rule-driven placement (self-assembly, tiling, CA-like growth)

- **Mass replication for free.** Once a seed and interaction rules are set, billions of identical units self-multiply; marginal "patterning cost" per instance collapses.
- **Intrinsic 3-D.** Colloids, DNA origami, block-copolymers, and metasurfaces form volumetric lattices, porous networks, or multilayered stacks without planar litho constraints.
- **Local error correction.** Embed legality/illegality in chemistry (binding energies, steric keys), add kinetic proofreading, and majority-vote tiles; errors can be detected and healed in situ.
- **Fractal/hierarchical structures.** Quadtree/Hilbert tilings and H-tree clock ribs emerge naturally; redundancy and routing are designed into the growth grammar.
- **Material diversity.** Plasmonic, photonic, phononic, catalytic, or memristive primitives can be co-grown; not limited to CMOS-compatible stacks.

Limits

- **Global registration.** Long-range drift, grain boundaries, and polycrystalline domains misalign features over distance without anchors.
- **Defectivity today.** Raw self-assembly defect rates are orders of magnitude worse than litho; without templating and repair, large arrays are unusable.
- **Programmable routing.** Arbitrary long wires, dense crossings, and precise vias are difficult purely bottom-up.
- **Reconfiguration control.** Switching or rewiring after growth requires additional stimulus (optical, thermal, electro-chemical) and careful isolation.

Hybrid leverage points (where rules + litho beat either alone)

- **Directed self-assembly (DSA).** Litho trenches/fiducials seed and phase-lock block-copolymers/DNA tiles; bottom-up fills between anchors with low defectivity.
- **Regular fabrics with top-down I/O.** Self-grown crossbars/CAMs or photonic crystals connected to litho power/clock/IO rails; yields programmable arrays at scale.
- **Built-in scrubbing.** Periodic "melt-and-heal" or ligand exchange acts like CA repeaters; litho sensors/actuators supervise scrub cycles.

5.3 Decision matrix: when to stay litho, when to go hybrid

Stay primarily litho when:

- **Tight overlay & timing closure** across many dissimilar layers is mandatory (complex SoCs, high-speed SerDes).
- **Irregular logic** dominates and area is routing-limited rather than device-limited.
- **Low defectivity** is non-negotiable and field repair is impractical (safety-critical control, medical implants without redundancy).
- **High-performance interconnect** with guaranteed impedance and EM compliance is required.

Go hybrid (litho anchors + rule-driven growth) when:

- **Topology is highly regular** (crossbars, CAMs, systolic arrays, memory-centric compute).
- **3-D density or spectral response** matters (photonic/phononic crystals, metamaterials, catalytic scaffolds).
- **Redundancy can mask defects** (TMR tiles, ECC, N-of-M sparing) and **local repair** is feasible (scrub/rebind).
- **Cost per replicated unit** must be minimized and iteration speed matters (new materials, exploratory architectures).
- **Fractal floorplans help** (H-tree clock/power ribs, quadtree containment, Hilbert backbones) and can be templated top-down while the body self-assembles.

Rule-only (rarely advisable)

- Acceptable only for **lab demos** or **noncritical metamaterials** where function is analog/statistical, not exact digital logic; expect significant yield variation and plan for over-provisioning.

Quick chooser (informal)

- **Need arbitrary logic + strict timing + scarce rework?** → Litho.
- **Need billions of identical cells + 3-D + can tolerate/recover defects?** → Hybrid.
- **Need tunable metamaterial response with coarse I/O?** → Hybrid (rules inside, litho couplers outside).

- **Exploratory, low-cost prototyping with new media?** → Start rules-first, add litho anchors as soon as arrays must scale.

Design implication. Treat lithography as the **skeleton** (registration, vias, clock/power/backbone, test points) and rule-driven growth as the **muscle** (dense, repeated, 3-D body). Compile to **regular macrocells** that the placer can map either to CA (simulation), to self-assembly recipes (materials), or to conventional standard cells (baseline), preserving architecture while swapping substrate.

6. Hybrid Blueprint: Anchors + Self-Multiplication

6.1 Coarse litho anchors: fiducials, power/clock rails, I/O

Goal. Provide global registration, long-range interconnect, and supervisory access while leaving bulk patterning to bottom-up growth.

- **Fiducials & graphoepitaxy guides.**
  Shallow, pitch-stable trenches and posts (50–200 nm pitch; AR 1–3) that phase-lock the self-assembling lattice. Place an H-tree of *metrology-visible* fiducials every 10–50 µm; expose in early metal (M0) so they survive downstream chemistry.

- **Power/clock "ribs."**
  Coarse rails (0.5–2 µm pitch) running as an H-tree across the die/wafer. Rails double as **local stimuli lines** (bias, heat, light) to gate growth steps and run "scrub" cycles. Include distributed shunt resistors to prevent hot-spot over-bias.

- **I/O islands (ports).**
  Bondable or TSV-terminated pads that break out: {supply, clock, scan, sense}. Surround each island with chemically inert moats to isolate wet steps. Provide **test multiplexers** that can connect any tile to a sense line for yield mapping.

- **Backbone vias.**
  Periodic via farms (e.g., every 5–20 µm) that later contact the self-assembled fabric's electrodes. Keep via capture pads oversized (≥3× expected overlay error) to tolerate growth drift.

Acceptance gates. Overlay ≤ 3 nm (3σ) across local fields; DC rail IR drop < 5% at max intended tile activity; fiducial contrast detectable through all wet/cure stacks.

6.2 Rule-driven growth: block-copolymers, DNA tiles, patchy nanoparticles

Common pattern: *Seed → Amplify → Lock → Passivate* with phase-stepped growth windows the litho ribs enforce.

- **Block-copolymers (BCP).**
  Use PS-b-PMMA (or high-χ BCPs) directed by trench guides. Tune χN and solvent anneal for target domain (lamellae/cylinders). After self-assembly, selectively remove one block to form **nanoporous masks**; back-fill with metal/oxide to form electrodes or insulators.
- **DNA origami tiles.**
  Program 10–30 nm tiles (double-crossover or origami rectangles) with **toehold sets** acting as allowed/forbidden keys (the "CA state alphabet"). Attach *addressable* metallization seeds (AuNPs, Pd) at specific vertices; use strand-displacement to correct mis-bindings (kinetic proofreading).
- **Patchy nanoparticles / colloids.**
  Janus or multi-patch particles with ligand patterns encoding neighbor selection. Surface chemistry yields **valence** and **angle constraints**; heat/light gates from the rails open/close specific bonds in phased steps.
- **Phase choreography (clocked chemistry).**
  Four-phase loop (ϕ0–ϕ3) mirroring our CA:
  ϕ0: nucleate (low supersaturation) → ϕ1: propagate (drive) → ϕ2: verify (proofread) → ϕ3: lock/passivate (covalent crosslink or ligand exchange).
  Litho ribs provide temperature/field/illumination modulation to keep the lattice phase-coherent across millimeters.

Acceptance gates. Domain period CV < 2%, grain size > 50 μm equivalent without dislocation, wrong-neighbor frequency < 10^{-4} before scrub.

6.3 Error control: kinetic proofreading, majority voting, scrub-and-heal steps

Local legality and repair are first-class, not afterthoughts.

- **Kinetic proofreading.**
  Multi-step binding with an *energy ladder*: E(legal) ≪ E(illegal). Introduce a reversible intermediate with a short lifetime (ATP-like fuel in wet systems; photo-isomerization in dry) so incorrect attachments preferentially fall off during ϕ2.
- **Majority tiles (TMR at materials level).**
  Triplicate functional sites (e.g., three junctions feeding one electrode). A **voter geometry**

(Y-merge with energy bias) ensures the majority structure templates the final conductive path; ambiguous triplets route into a **neutral sink** pad reworked at scrub.

- **Sentinel markers.**
  Include "error dye" ligands or plasmonic tags that bind to under-coordinated motifs. During ϕ2, excite optically and read out through the I/O islands for *in-situ* defect maps.

- **Scrub-and-heal.**
  Periodic, global but **phase-staggered** cycles: gentle solvent/heat pulse + light toehold activation that releases flagged tiles; reflow, then re-bind under ϕ0–ϕ1. For metals, use **electrochemical polishing** windows on the ribs to open/close local deposition selectively.

- **Containment perimeters.**
  Fractal (Sierpinski-like) guard bands with high binding energy that **absorb defect propagation**. They also act as cut-lines for later isolation if a region remains sick.

Acceptance gates. Post-scrub defectivity < 10^{-8} per functional site (crossbar junction or equivalent) on 1 cm^2; > 99.99% of sentinel events cleared in one scrub; no growth beyond guard bands.

6.4 Metallization and vias: turning fabrics into logic/memory arrays

From pretty lattices to programmable devices.

- **Selective metallization.**
  Use the self-assembled mask to plate **orthogonal electrode sets**:
  – Layer A (word lines) via electroless Cu/Co through DNA/BCP masks.
  – Layer B (bit lines) orthogonal, isolated by ALD dielectrics between scrubs.
  – Optional **threshold materials** (e.g., Ag:Si for memristive filaments) at junctions by site-specific seeds.

- **Via capture & alignment.**
  Oversized capture pads on BEOL connect to the self-assembled electrode buses. Use **self-aligned via etch** that keys off the dense lattice, then litho defines the coarse via farm that lands anywhere within the statistical window.

- **Programmable junctions.**
  At crossings:
  – **Resistive memory:** ionic filament formation with forming pulses through power ribs.
  – **Tunnel/diode:** asymmetric metals/oxides grown by sequential infiltration synthesis.

– **Photonic/phononic:** fill patterns with high-index or stiff inclusions to set bandgaps; top-down couplers inject/extract signals.

- **Passivation and planarization.**
  Low-k or polymer caps to freeze the lattice; light CMP if required to mate with top metals; maintain *re-entry* capability for later scrubs in designated windows.

Acceptance gates. Line resistance and junction IV within design spec (3σ); via yield > 99.999%; leakage floor below ECC threshold; cross-talk < budget under AC bias.

6.5 First targets: crossbars, CAMs, photonic/phononic crystals, neuromorphic grids

Pick functions that love regularity, tolerate redundancy, and benefit from 3-D.

- **Resistive crossbars (MxN).**
  Why: Maximum repetition; ECC hides sparse defects; ideal for in-memory dot-products and key-value tables.
  Spec: M,N = 10^3–10^5 per tile; ECC with product codes or staircase codes; periodic majority-tile voters on word/bit segments.
  Metrics: Post-scrub bad-junction rate < 10^{-7}, analog linearity for MAC within 1% after calibration.

- **Content-addressable memories (CAM/TCAM).**
  Why: Bit-parallel match lines map naturally to dense regular electrodes.
  Spec: Dual-rail match cells; local refresh (scrub) every 10^6 ops; spare rows/columns with Morton-code remap.
  Metrics: Match error rate < 10^{-12}/op with ECC; update energy < CMOS within same footprint due to short wires.

- **Photonic/phononic crystals.**
  Why: Bandgap control thrives on periodicity; 3-D stacking improves spectral richness.
  Spec: Lattice constants 100–500 nm (photonic) or 0.5–5 µm (phononic); litho couplers/gratings at anchors.
  Metrics: Bandgap Q-factors within 5% of sim across cm-scale; tunability via local actuation rails.

- **Neuromorphic grids (memristive or phase-change).**
  Why: Analog/statistical computing tolerates residual disorder; local learning uses short wires.
  Spec: STDP-like update windows gated by ribs; TMR readout on critical decision lines; periodic re-leveling via scrub pulses.

Metrics: Task accuracy within 1–3% of ideal with 5–10% device variability; stability over 10^9 updates.

Design takeaway. Treat lithography as **scaffold and supervisor**—setting the frame, power, clock, I/O, and inspection—while rule-driven growth **fills the body** with ultra-dense, regular fabrics that can be **repaired in place**. The four-phase chemical "clock," majority geometries, and sentinel feedback close the loop between **self-assembly** and **system engineering**, turning beautiful lattices into **serviceable arrays** you can compile to and operate at scale.

7. Minimal Prototypes

7.1 CA demo: 64×64 leaf, ripple adder, fan-out, DFF pipeline, fault injection & repair

Objective. Prove the engineerability of the CA rule set—clean wires, timing, storage, flow control, and local fault handling—on a single leaf that can be tiled later.

Scope & targets

- **Leaf size:** 64×64 cells (T0–T3 clock tiling uniform).
- **Library used:** {INV, NAND2, XOR2, DFF, F/M, R, L, Router-μ, GALS shim}.
- **Designs inside leaf:**
    1. **4-bit ripple-carry adder** (RCA4) with dual-rail I/O, one result per 6ϕ.
    2. **Fan-out tree**: 1→4 splitter driving four XOR2s (legal F/M discipline).
    3. **DFF pipeline**: 8-stage shift register with VALID/READY handshake.

Layout plan

- **Quadrants:** Q0—adder, Q1—fan-out test, Q2—pipeline, Q3—router loopback.
- **Tracks:** 4 signal tracks per row, R every 10 cells; alert rail per column.
- **Ports:** N/E/S/W standardized; loopback on E-side for latency probes.

Test protocol

1. **Functional sweep.** Cycle all 16 input pairs into RCA4; compare outputs bitwise; log latency histogram (goal: 6ϕ ±0).

2. **Throughput sweep.** Drive VALID at 1 token/ϕ; downshift READY to induce back-pressure; ensure no token loss or illegal merges; measure sustained ops/ϕ.
3. **Fan-out legality.** Arm F tree; randomly block one branch (READY low); verify global stall until both READY high; assert E if violated (should be 0 in clean run).
4. **Pipeline integrity.** Inject pseudo-random dual-rail pattern; read back after 8 stages; BER target: 0 with Rs every 8 cells.
5. **Fault injection.**
    - **Transient:** flip one cell to I mid-rail; expect local E, upstream stall, watchdog SCRUB, resume within ≤50ϕ.
    - **Permanent:** stuck-E cell; quadtree parent (mocked within leaf) isolates region; router detours via alternate track; progress resumes with ≤2× latency for affected nets.

Instrumentation & acceptance

- **Counters:** VALID/READY toggles, E events, scrub cycles, average ϕ latency.
- **Waveform taps:** four observation points per net (pre/post R, boundary).
- **Pass if:** (i) 100% functional for RCA4; (ii) no illegal dual-rail states; (iii) transient faults recovered <50ϕ; (iv) permanent fault contained with forward progress.

7.2 Materials demo: directed self-assembly with fractal seeds and ECC tiles

Objective. Show that hybrid, rule-driven growth can achieve low-defect regular fabrics with built-in error signaling and repair.

Bill of materials (exemplar choices)

- **Substrate:** Si/SiO_2 with graphoepitaxy trenches (100–150 nm pitch) in a 4×4 **quadtree seed** layout (each child a 200×200 µm field).
- **Self-assembly:** High-χ BCP (PS-b-PMMA, χN tuned for 12–20 nm domains) or DNA origami tiles (30 nm pitch) with toehold sets $\{T_0,T_1,T_2\}$.
- **Metals:** Electroless Cu/Pd for electrodes; ALD Al_2O_3 for isolation.
- **Sentinels:** Fluor tags bound to under-coordinated motifs; quenched after repair.

Process choreography (mirrors ϕ0–ϕ3)

1. **ϕ0 Nucleate:** Load BCP/tiles into quadtree trenches; mild anneal (solvent or thermal) under uniform rib bias.
2. **ϕ1 Propagate:** Increase drive (temperature/field) to extend domains; activate patch ligands T_o.
3. **ϕ2 Proofread:** Pulse light/chemical fuel to enable strand displacement or selective debonding; expose sentinel readout through I/O islands; map defects.
4. **ϕ3 Lock/Passivate:** Crosslink legal bonds; ALD dielectric cap; quench sentinels.

ECC macro-geometry

- **Majority tiles:** 3 parallel domain lines merge into one capture pad; mis-majority shunted to a neutral sink (visible electrically during test).
- **Sierpinski guard:** High-binding perimeter around each quadtree child; contains grain boundary spread and defines later cutlines.

Test structures & metrics

- **Crossbar coupon:** 256×256 junctions per child; post-scrub IV sweeps over 1% sample uniformly distributed.
- **Yield mapping:** Electrical probe via I/O islands; interpolate to full map.
- **Targets:**
    - Pre-scrub defectivity ≤10^{-4}/junction; **post-scrub ≤10^{-7}**.
    - Majority voters correct ≥99.99% of single-line defects.
    - Grain size > 50 µm; overlay of lattice to anchors within ≤15 nm (3σ).

Repair loop

- If sentinels > threshold in a child: freeze neighbors, **localized scrub** (heat/solvent/optical), re-anneal ϕ1, re-lock ϕ3, re-probe.
- If persistent: **isolate child** at guard band; mark for spare substitution in 7.3.

7.3 Integration demo: litho H-tree + self-assembled array + measured yield

Objective. Close the loop: register bottom-up fabric to top-down rails, expose programmable function, and quantify yield/repair at the system level.

Die plan (mm-scale)

- **Anchors:** H-tree **power/clock ribs** at 1 µm pitch feeding 4×4 quadtree fields (from 7.2).
- **I/O islands:** 16 ports around perimeter (word/bit buses, bias, scan, sense).
- **Via farms:** Capture pads every 10 µm bridging to crossbar word/bit electrodes.

Functional blocks

- **Block A (Crossbar-MAC tile):** 1k×1k resistive crossbar, row/col decoders in metal, per-tile ECC (product code), and calibration DACs.
- **Block B (CAM slice):** 512 entries × 64-bit TCAM cells; match lines with TMR voters; spare rows/cols (N-of-M).
- **Control:** Microcontroller or FPGA off-chip driving scan/measure sequences; rib control for ϕ-phased "scrub" pulses.

Bring-up sequence

1. **Continuity & shorts.** Kelvin measurements of rails/vias; reject if IR drop >5%.
2. **Structural scan.** Sentinel fluorescence map; electrical BIST of majority tiles.
3. **Scrub pass 1.** Global ϕ2 proofread + relock; re-BIST.
4. **Spare mapping.** Identify persistent bad rows/cols; remap address tables (Morton codes) to on-die spares; store map in nonvolatile fuses/registers.
5. **Functional tests.**
    - **Crossbar MAC:** Random vectors; compare analog MAC vs golden within 1% after calibration.
    - **CAM:** Random queries; **target $<10^{-12}$** match error per op with ECC; measure energy/op.

Measured outputs (reportables)

- **Yield curves:** Pre/post scrub; post spare-map.
- **Defect pareto:** Line opens, shorts, via misses, voter disagreements.

- **Performance:** Bandwidth (rows/s), energy per MAC/lookup, calibration time.
- **Reliability:** Drift over 10^6–10^8 ops; periodic mini-scrub effectiveness.

Acceptance criteria

- **Connectivity:** Via yield > 99.999%.
- **Functionality:** ≥ 99% of tiles operational post-scrub and remap; crossbar MAC error ≤ 1% rms; CAM false-match rate ≤ 10^{-12}/op (with ECC).
- **Serviceability:** Localized scrub recovers ≥ 90% of flagged defects; isolate-and-spare restores full function with ≤ 5% area overhead.
- **Reproducibility:** Across ≥ 3 dies, variance of key metrics ≤ 10%.

Takeaway. These three prototypes ladder from **rule-correct CA logic** (7.1), to **low-defect self-assembled fabrics with built-in repair** (7.2), to a **hybrid, measured system** where lithographic anchors supervise a dense, rule-grown array (7.3). Passing the acceptance gates establishes a credible path from paper architecture to scalable hardware.

8. Field-Native Computing: Lessons from Ultra-Weak Media

8.1 MVIS (minimum viable intelligent substrate) requirements

To compute in media that couple only weakly to us (or to ordinary matter), the substrate must satisfy four non-negotiables:

- **Statefulness.** Long-lived, addressable degrees of freedom (DOFs) with metastable wells and separation of timescales: write/erase time << retention time. In fields, candidates are phase domains, bound states, topological charges, or trapped modes.
- **Controllability.** A way to bias transitions among states with small, localized drives (boundary conditions, parametric pumping, weak potentials) that do not destroy coherence. Control bandwidth can be tiny; what matters is specificity.
- **Transport.** Mechanisms to move information without catastrophic dispersion: group-velocity windows, soliton rails, advection along controlled flows, or protected edge modes. Transport must compose (store → move → compute → store) without cumulative error blow-up.

- **Error economics.** Native suppression and correction: energy gaps between legal/illegal motifs, topological protection against small perturbations, and redundancy patterns that permit majority voting or self-healing. Landauer/adiabatic accounting must be favorable at the ambient noise floor.

Operational corollaries:

- **Clocking without a crystal.** Use phase windows or parametric cycles as a four-phase "chemical/field clock" (seed, propagate, verify, lock).
- **Boundary contracts.** Every region that exchanges information does so with explicit handshakes (ready/valid analogs) implemented as phase or amplitude tags.
- **Observability.** Even if the medium is dark, at least one messenger (gravitational, portal mixing, or proxy field) must carry telemetry to verify correctness.

8.2 Candidate media: ultralight bosonic fields, SIDM fluids, dark photons, PBH clouds

We treat each as a computing *material* with characteristic DOFs, control knobs, transport, and failure modes. (Where cosmic control is infeasible, use laboratory analogs to learn the principles.)

- **Ultralight bosonic fields (axion-like; "fuzzy" DM).**
  DOFs: macroscopic phase of a coherent scalar, soliton cores, interference fringes, oscillons.
  Control knobs: boundary tides; periodic drives near 2*f_c (parametric pumping at twice the Compton or cavity frequency); weak mixing with photons in strong B fields (lab analog).
  Transport: phase fronts, soliton glide, core–halo breathing modes.
  Failure modes: dispersion, dephasing, modulational instability beyond safe amplitude.
  Lab analogs: cold-atom BECs in optical lattices; nonlinear optical cavities with Kerr media.

- **Self-interacting dark-matter (SIDM) fluids.**
  DOFs: density waves, shocks, vortices; long-lived caustics in mildly collisional regimes.
  Control knobs: slowly varying gravitational potentials (bars, rings) or lab-fluid analogs with tunable viscosity.
  Transport: advection along streamlines; soliton-like pulses in weakly dissipative channels.
  Failure modes: turbulence and shock dissipation; sensitivity to boundary roughness.
  Lab analogs: shallow-water, plasma, or active-matter flows engineered to match Reynolds and interaction parameters.

- **Dark photons / hidden-sector plasmas.**
  DOFs: vector potentials and plasma modes; Bernstein–Greene–Kruskal-like trapped waves in low-collision regimes.
  Control knobs: kinetic mixing windows; cavity resonances; external periodic fields (lab).
  Transport: guided modes in effective "waveguides" set by density profiles; mode conversion.
  Failure modes: Landau damping; mode crowding near cutoffs.
  Lab analogs: RF/optical photonic lattices, metamaterials emulating mixed media.

- **Primordial black holes (PBHs) with boson clouds (superradiance).**
  DOFs: quantized bound states around spinning BHs; discrete mode spectra coupled to spin.
  Control knobs: spin history and accretion (not engineerable by us, but observable); timing in lab analog ring-down cavities.
  Transport: mode beating and gravitational emission; information in spectral occupancy and phase.
  Failure modes: nonadiabatic spin changes, cloud depletion.
  Lab analogs: superradiant-like amplification in rotating fluids or optical ring cavities.

Design intuition across media:

- Favor **coherent, weakly dissipative** regimes where nonlinearity exists but is controlled.
- Encode in **topological or phase** variables first; use amplitude only for handshakes or error flags.
- Employ **hierarchies**: local DOFs for fast logic; global, slow DOFs for clocking and memory.

8.3 Logic primitives in fields: solitons, oscillons, vortices, caustics as "gates"

We map field excitations to the roles played by wires, gates, latches, and routers in silicon/CA. The emphasis is on *composable motifs* with explicit timing and error handling.

- **Wires = guided modes / channels.**
  Construct quasi-1D conduits by shaping refractive index, density, or potential so that a specific mode propagates with minimal loss. In ULDM/BEC analogs, use index rails from weak potentials; in plasmas/photonic lattices, use band-gap guidance.
  Contract: one pulse per temporal slot; adjacent slots separated by guard time and a regeneration section.

- **Signals = soliton/oscillon pulses (dual-rail analog).**
  Represent bit-0 and bit-1 by two phase-locked families of pulses (dual-rail in phase space, not voltage). Solitons self-heal after weak collisions; oscillons act as localized

carriers that can be captured and re-emitted.
Regeneration: periodic sections that rephase pulses using weak synchronous pumping (adiabatic, low dissipation).

- **Gates = controlled collisions in prepared junctions.**
  At Y or X junctions engineered to conserve invariants, specific two-pulse encounters deterministically map to outputs (collision computing).
  Examples:
    - NAND/XOR via phase-conditioned crossings: simultaneous arrival produces a mode-converted output; single arrivals pass through.
    - Majority/C-element via tri-merge cavities that output only if incoming phases agree within tolerance; else decay to a sink.
      Legality masks: junctions include "forbidden" phase zones that dump illegal superpositions into lossy reservoirs (error sink) instead of contaminating the network.
- **Latches = phase traps / bound-state buckets.**
  Create small potential wells or defect modes with two stable phase occupations. A write pulse toggles occupancy; readout emits a probe that acquires a phase shift only if the trap is occupied (dispersive read). Master–slave pairing with phase windows prevents transparency.
- **Fan-out / fan-in = mode splitters and combiners.**
  Adiabatic Y-splitters duplicate a pulse into two rails with fixed amplitude ratio; legality requires both outputs to be "empty" windows. Combiners implement OR/majority in phase space; ambiguous superpositions route to a reservoir and raise an error flag on a side channel.
- **Routers = resonant switches.**
  Small cavities whose resonance toggles under a slow control bias route incoming pulses to different outputs (crossbar elements). Low-rate control maintains energy efficiency; data pulses stay fast relative to control.
- **Clocks = parametric cycles.**
  Four-phase loop: seed, transport, collide, sanitize. Implemented by weak global modulation (e.g., of nonlinearity or potential depth) so that gate regions are "transparent" except during the collide window. This is the field analog of T0..T3 tiles.
- **Error signaling and repair.**
  Every gate emits a faint sideband when an illegal event occurs (e.g., both rails occupied

or forbidden phase); sidebands are trapped by **sentinel resonators** that accumulate error energy and periodically release a scrub pulse. Scrub cycles locally reset phases, analogous to CA repeaters and sanitation passes.

- **Long-distance comms = advection and conversion.**
  For kilometer-to-galaxy scales (conceptual), rely on slow advection of robust structures (soliton trains, caustics) and encode with **low-entropy codes** (repetition, majority, convolutional constraints). At domain boundaries convert between mode families using engineered heterojunctions.

Performance envelopes (qualitative):

- **Energy/bit.** Approaches adiabatic/reversible limits if regeneration is gentle and sinks are rarely triggered.
- **Rate.** Determined by the shortest safe separation between pulses and the Q of junctions; often orders of magnitude below electronic speeds but vastly lower dissipation.
- **Scale.** Exceptional reach because transport losses can be engineered small; redundancy handles sparse defects.

Takeaway. The same engineering primitives that made our CA fabric viable—dual-rail discipline, four-phase timing, legal/illegal masks, regeneration, voters, and hierarchical routing—translate into field-native form when you reinterpret “wires” as guided modes, “gates” as controlled collisions, and “latches” as phase traps. Even if cosmic media are forever out of reach, lab analogs let us test these ideas, giving us recipes for computing in the extreme low-coupling, low-dissipation regime that future embodied meshes will increasingly require.

9. Seeding Protocols (Highly Speculative, Lab-First)

9.1 Parametric writing near Compton or cavity frequencies (lab analogs)

Goal. Demonstrate controlled write/erase of long-lived field states (phase domains, solitons, trapped modes) in laboratory media that emulate ultra-weak, coherent substrates.

Platforms

- **BEC/optical lattice** (Rb or Na): tune g via Feshbach; lattice depth V0 in 4–12 E_r; target weak nonlinearity.
- **Nonlinear optical cavity** (Kerr ring or microresonator): pump near resonance; dispersion managed for soliton existence.

- **Exciton-polariton lattices / photonic waveguide arrays**: discrete, low-loss channels.

Protocol A (BEC, parametric pump)

1. Prepare ground state in shallow lattice; measure background phase noise S_phi(f).
2. Pick target mode frequency f_0 (lowest cavity/box mode). Drive **parametrically** at f_p = 2 f_0 with small depth modulation: V(t) = V0 * [1 + epsilon * cos(2 pi f_p t)], epsilon ~ 0.01–0.05.
3. Seed a localized phase step (pi/2) with a brief, off-resonant pulse; hold the parametric pump for tau_write.
4. Switch to hold (no pump) and track the seeded domain lifetime tau_ret via interferometry.
5. Erase by phase-conjugate pulse at f_0 or by adiabatic ramp of V0 to suppress the mode.

Protocol B (Kerr cavity, comb writing)

1. Pump the cavity slightly below threshold; detuning Delta < 0.
2. Apply a weak amplitude modulation at f_p ~ 2 f_FSR to trigger parametric sidebands; grow into a single dissipative soliton.
3. Encode a bit by soliton presence/absence or by relative phase of two solitons separated by T_slot.
4. Regenerate with periodic, low-amplitude “tick” pulses synchronized to the cavity round-trip (acts like an R repeater).

Acceptance metrics

- Write time tau_write << retention time tau_ret (target tau_ret/tau_write > 10^3).
- Minimal collateral heating: delta T < threshold that would change dispersion/nonlinearity more than 1%.
- Deterministic erase with BER_erase < 10^-6 over N cycles.

9.2 Phase-encoded, fractal-renormalizable codes for longevity

Design idea. Store information in phase patterns that re-instantiate themselves after partial loss, using a hierarchical (quadtree/Hilbert) structure and dual-rail phase logic.

Code elements

- **Dual-rail phase:** two phase families {phi_A, phi_B} with separation ~ pi/2; 0 = token on A, 1 = token on B.
- **Fractal scaffold:** tiles organized quadtree-style; each parent carries a parity/checksum over its four children.
- **Hilbert addressing:** traversal order for refresh and readback preserves locality.

Write algorithm (sketch)

1. Map payload bits to leaf tiles along a Hilbert curve.
2. For each 2x2 sibling group, compute a local parity p = XOR(children). Store p in the parent's phase bucket.
3. Repeat up the tree to depth D.
4. Emit a low-duty "tick" that re-phases leaves to canonical phi_A/phi_B (combats drift).

Repair (renormalization)

- On read, if any child in a 2x2 set is ambiguous, recover it from the other three and the stored parity at the parent.
- If a parent parity is ambiguous, ascend one level and use grandparents; if ambiguity persists beyond depth K, mark the region for re-write.

Code parameters

- Tile size L_tile (spatial) and slot time T_slot (temporal) set the refresh horizon.
- Choose depth D so that diffusion length over refresh interval L_diff < L_tile.
- Redundancy rate R ~ (4^D - 1)/(4^D) (parity per 2x2 block). Typical D=3..4 balances overhead and robustness.

Targets

- Correct up to 1 missing/ambiguous child per 2x2 without escalating.
- With random erasures p_e, probability of uncorrectable block falls as O(p_e^2) after one renormalization pass.

9.3 Energy and entropy: reversible/adiabatic drives, engineered sinks

Principle. Keep writes near the adiabatic limit; only illegal or ambiguous events should dissipate energy into designated sinks (scrub reservoirs).

Adiabatic write

- Ramp control parameters on timescale tau_ramp >> 1/f_0 to avoid exciting unwanted modes.
- Use counter-diabatic “shortcuts” only if they do not broaden spectra into lossy bands.

Regeneration

- Insert low-amplitude, periodic re-phase pulses that project states back onto the code manifold (dual-rail phases). Energy per tick E_tick chosen so that E_tick << E_bit but sufficient to overcome measured phase diffusion D_phi.

Engineered sinks

- Place lossy side-cavities or detuned reservoirs at junctions where illegal superpositions appear; couple weakly (kappa_sink) so legal traffic is undisturbed.
- Scrub cycles briefly increase kappa_sink and apply a shaped pulse to pull population out of forbidden subspaces.

Thermodynamic accounting

- For each write/refresh/scrub step, track:
  E_in (control work), E_store (free energy in the encoded mode), E_diss (to sinks/heat).
- Targets: E_diss/E_in minimized for legal operations; E_diss spikes only during error handling.
- Empirical Landauer budget: verify k_B T ln 2 bounds are not exceeded by orders of magnitude in nominal cycles.

9.4 Safety valves: designs that decay to noise without sustained drive

Fail-safe requirement. If control signals cease or drift beyond tolerances, the encoded structure must naturally relax to an innocuous baseline (no runaway attractors).

Mechanisms

- **Subcritical nonlinearity:** choose operating points below self-oscillation thresholds; no free lasing/parametric runaway.
- **Metastability with leak:** add a small, controlled leakage gamma_leak so that in the absence of ticks the memory decays with time constant tau_leak (set longer than operational refresh, shorter than environmental risk horizon).
- **Bound reservoirs:** engineered sinks that cap energy and phase density; any excess is drawn off passively.

Tripwires and watchdogs

- **Envelope monitors:** detect growth in forbidden bands; trigger global dampening (increase kappa_sink and lower drive).
- **Parity sentinels:** if renormalization fails at level K twice consecutively, freeze writes to that region and issue a maintenance request.
- **Quench mode:** single command (or automatic on control-loss) ramps detuning to a safe, off-resonant point; all excitations decay with tau_quench.

Validation tests

- Pull-the-plug: abruptly remove drives; verify decay to baseline in < tau_safety while no spurious emissions occur.
- Drift injection: detune control by delta over time; confirm watchdogs quench before entering unstable regions.
- Black-start: after full decay, re-apply nominal control; demonstrate clean re-seeding without latent hysteresis.

Governance note. All field-native protocols must be published with null-test plans and quench sequences. Default on failure is “return to noise,” not “persist in unknown state.”

Takeaway. Seeding in ultra-weak media is less about “writing bits fast” and more about **writing bits that calmly survive**, **heal when nicked**, and **disappear harmlessly** if unattended. Parametric writing gives you precise handles; fractal codes give you longevity; adiabatic control keeps entropy in check; and safety valves ensure reversibility. These lab-first recipes translate our CA discipline (dual-rail, phases, regeneration, error sinks) into the physics of waves and fields.

10. Observational Tests (Falsifiable)

10.1 Algorithmic-structure search: mid-compressible motifs in pulsar timing, lensing, streams

Hypothesis. If a dark-sector substrate carries engineered information, some time/space series that *should* be stochastic will exhibit **mid-compressible** structure: neither white noise nor trivially periodic.

Datasets.

- **Pulsar timing:** post-fit residuals from millisecond pulsars (weekly–biweekly cadence, multi-year baselines).
- **Microlensing:** event-rate time series and impact-parameter distributions from wide-field surveys.
- **Stellar streams:** 1-D density/phase-space profiles along cold streams; gap sizes and spacings.

Pipeline.

1. **Denoise & whiten** with standard astrophysical models; preserve residuals.
2. Compute **structure diagnostics** on sliding windows and globally:
    - Lempel–Ziv complexity (LZ78), **normalized compression distance** (NCD).
    - **Spectral flatness** and **multitaper entropy**.
    - **Permutation entropy** and **ordinal pattern** distributions.
    - **Automaton fits:** minimal DFA size fitting symbolized sequences (via coarse quantization).
3. Establish **null ensembles** by bootstrapping, phase randomization, and surrogate data with identical power spectra.
4. Flag windows that fall in a **mid-compressible band**: e.g., NCD $\in (0.2, 0.6)$ *and* spectral entropy $\in (0.6, 0.85)$.

Controls.

- Instrumental systematics templates (clock errors, scanning laws).
- Known astrophysical quasi-periodic sources (binaries, bars) to set exclusion masks.

Decision rule.

- Pre-register thresholds; require **replication across targets** (≥3 pulsars or ≥2 streams) and **stability under detrending choices** to claim an anomaly.

10.2 Cross-messenger coincidences and time-locking

Hypothesis. An engineered signal would hedge against noise by **co-designing redundancy** across independent channels (e.g., timing + lensing), with **time-locked** motifs.

Channels & features.

- **PTA residual motifs ↔ microlensing rate modulations ↔ stream gap spacings** within the same sky sectors and epochs.
- Optional fourth messenger: **weak-lensing shear E/B-mode anomalies** at matching angular scales.

Pipeline.

1. Convert each channel to **symbol sequences** (e.g., up/down/flat, gap/no-gap, high/low shear) with consistent temporal or angular binning.
2. Use **cross-recurrence plots** and **transfer entropy** to test directed associations.
3. Compute **delay-embedding correlations** to allow for known light-travel/propagation lags; scan a bounded lag window (e.g., ±5 years).
4. Control the **look-elsewhere effect** by Bonferroni or false-discovery–rate procedures over lag and location trials.

Decision rule.

- A detection requires: (i) peak cross-information above pre-registered threshold; (ii) **phase coherence** over ≥3 cycles/bins; (iii) **geometric consistency** (same sky footprint to within survey resolution).

10.3 Mode fingerprints: narrow lines from boson clouds and core–halo beats

Hypothesis. Field-native structures (e.g., boson clouds around compact objects, or core–halo oscillations in ultralight fields) produce **narrow spectral lines** or **avoided crossings** that persist in time.

Targets.

- **Compact-object spectra:** quasi-normal modes, continuous narrow-band features in timing or strain power spectra.
- **Halo interiors:** low-frequency **breathing/beat modes** in kinematic or lensing residuals of dwarf galaxies and LSB spirals.

Pipeline.

1. Build **mode dictionaries** from simulations (axion mass grid, self-interaction strengths, rotation/spin parameters). Record predicted frequency ratios and linewidths (Q factors).
2. Perform **matched filtering** / line searches with **multi-harmonic templates**; allow slow chirps consistent with secular evolution.
3. Require **fixed frequency ratios** across harmonics (e.g., f_2/f_1 within 1–2% of template), or characteristic **doublets/triplets** from avoided crossings.
4. Track **temporal coherence**: Q ≥ Q_min over a pre-registered observing span; reject transient RFI/systematics via multi-instrument coincidence.

Decision rule.

- A candidate survives if: (i) ≥3 harmonically related lines; (ii) linewidths match predicted damping; (iii) no known astrophysical confounder fits better **without** extra parameters (information criterion win).

10.4 Negative results as constraints on dark-sector dynamics

Purpose. Absence of structure is informative. We translate nulls into limits on coherence, interaction strength, and control bandwidth of putative dark media.

Constraint construction.

- **Algorithmic nulls → decoherence bounds.** If all series are **maximally compressible (noise-like)** to within ε, set upper limits on **coherence time** τ_c and **phase diffusion** D_ϕ of field DOFs: τ_c < τ⋆(ε), D_ϕ > D⋆(ε).
- **No coincidences → coupling limits.** Lack of cross-messenger time-lock implies an upper bound on **inter-channel coupling** κ (e.g., axion–photon mixing, effective gravitational modulation depth).

- **No lines → mass/self-interaction boxes.** Exclude regions in (m, g_self) where predicted Q and amplitudes would have been detectable at the achieved sensitivity.

Reporting.

- Publish **exclusion plots** with clearly stated assumptions (source populations, sky coverage, cadence, noise). Provide **open pipelines** and synthetic-signal injection studies to document sensitivity.

Guardrails.

- **Pre-registration** of statistics and thresholds to avoid p-hacking.
- **Blinding**: inject undisclosed synthetic signals to validate detection efficiency; unblind only after pipeline freeze.
- **Replication** across instruments/surveys before claims.

Value of nulls. Tightens priors for dark-sector models, informs lab-analog parameter choices (target Q, drive depth, refresh rates), and guides instrument design (cadence, spectral resolution) for the next round of tests.

Bottom line. These tests are **binary** in spirit: either mid-compressible structure, time-locked redundancy, and stable mode fingerprints appear with pre-registered significance, or they don't—and both outcomes move the science forward.

11. Governance, Ethics, and Risk Management

11.1 Prime directive for cosmic substrates: non-interference and reversibility

Principle. Treat cosmic media—especially dark-sector candidates—as shared, nonrenewable commons. Default posture: *observe without perturbing; prototype only in lab analogs; any sky-facing action must be reversible by design.*

Operational rules

- **Reversibility-first design.** Any field or material protocol must have a **quench path** (detune, cool, depump) that returns the medium to a baseline state on a bounded timescale. Require proof-of-quench in analogs before observations or proposals move forward.

- **No net state change without consent.** “Consent” = demonstrated scientific necessity + community review + formal risk approval. Passive sensing and algorithmic analysis are preferred over active driving; astrophysical “natural experiments” substitute for deliberate excitation.
- **Minimal coupling.** Use the weakest feasible probes; ban proposals that rely on large-scale gravitational sculpting, persistent EM injection into astrophysical systems, or irreversible chemical/thermal alterations.
- **Boundary of influence.** Predefine spatial/temporal containment ($\Delta\Omega$ on the sky; Δt in years). If predicted influence leaks outside bounds under worst-case modeling, the action is disallowed.
- **Fail-quiet defaults.** On anomaly or telemetry loss, systems must auto-enter **fail-silent** (no emission, no drive) rather than fail-loud.
- **Third-party stewardship.** Establish an independent **Ethics & Risk Board (ERB)** with veto power; publish meeting minutes. Conflicts of interest (instrument PIs, funding bodies) must be disclosed and recused.

Red lines (categorical prohibitions)

- Irreversible injection of energy/momentum into celestial systems.
- Intentional modulation of signals used by safety-critical space assets (e.g., GNSS, deep-space comms).
- Attempts to “seed” cosmological-scale structures outside validated lab analogs.

11.2 Publication norms: null tests, preregistration, open data

Objective. Prevent p-hacking, selection bias, and unfalsifiable claims; maximize reproducibility and community oversight.

Pre-registration & analysis plans

- **Hypotheses & metrics.** Register target statistics (e.g., Lempel–Ziv windows, line Q thresholds), sky regions, lag scans, and stopping rules before touching data.
- **Synthetic injections.** Define amplitudes, frequencies, and densities of hidden injected signals to calibrate sensitivity. Only after pipeline freeze may teams unblind.
- **Multiple comparisons.** Declare correction methods (FDR/Bonferroni) and trial counts in advance.

Open pipelines & artifacts

- **Code & configs.** Release versioned containers (hash-locked), notebooks, and config files that reproduce figures end-to-end.
- **Data availability.** Provide raw or minimally processed residuals with masks and calibration metadata, subject to survey policies. If raw release is impossible, release **surrogates** sufficient to rerun the statistics.
- **Provenance logs.** Auto-generate machine-readable run logs (git SHAs, parameter diffs, environment fingerprints) for every figure and table.

Nulls as first-class results

- **Negative catalogs.** Publish "nothing-found" reports with achieved sensitivities and exclusion regions; deposit alongside positive claims.
- **Replication tracks.** Reserve space in journals and conferences for independent re-analyses; positive claims require **multi-instrument** replication to graduate from "candidate" to "detection."

Transparency incentives

- **Credit policies.** Citations for dataset curators and pipeline maintainers; badges for full reproducibility.
- **Embargo discipline.** Coordinated releases to avoid "salami slicing" and media overclaiming.

11.3 Terrestrial parallels: refusal protocols, sabbath schedules, fault-isolation in embodied meshes

Premise. The same governance instincts we apply to cosmic substrates should shape Earth-scale, embodied compute meshes (CA fabrics, hybrid arrays, field-native labs).

Refusal protocols (safe defaults)

- **Refuse-by-default interfaces.** Critical operations (overclocking leaves, disabling scrubs, writing irreversible fuses) require multi-party approval and cryptographic quorum (M-of-N keys).
- **Capability bounding.** Runtime enforces **policy envelopes**: max tick rates, max injection bandwidth, max error budget. Requests outside the envelope return structured refusals with rationale.

- **Intent verification.** For automated agents, require machine-checkable proofs (or attestations) that requested actions satisfy safety invariants (no cross-quadrant spill, no bypass of voters).

Sabbath schedules (programmable rest)

- **Cyclic quiet windows.** Regular, enforced downtime where arrays enter low-power **observe-only** mode: scrub, re-calibrate, and run BIST. Human review windows coincide with sabbath to catch drift and debt.
- **Adaptive cadence.** Increase sabbath frequency when error rates or thermal telemetry exceed thresholds; relax when healthy. All overrides are logged and reviewed post hoc.

Fault isolation & graceful degradation

- **Containment by construction.** Quadtree boundaries, Hilbert backbones, and explicit VALID/READY contracts ensure faults localize to a leaf/quadrant.
- **Tiered responses.** (1) Stall ingress; (2) drain; (3) scrub; (4) isolate; (5) remap to spares; (6) degrade service-level objectives rather than crash.
- **Forensic hooks.** Immutable logs (append-only) for E-alerts, watchdog trips, and policy override events; support postmortems without halting the system.

Human-in-the-loop governance

- **Two-person rule** for policy changes and disabling safety valves.
- **Red teams** simulate adversarial misconfigurations and insider mistakes; publish drills and outcomes.
- **Ethical training** for operators: checklists, tabletop exercises, and “no blame, high learning” incident reviews.

Socio-technical guardrails

- **External audit.** Annual independent assessments of safety posture, with public summaries.
- **Community charters.** Shared norms across labs/vendors (e.g., “Open Quench Protocols,” “Nulls First”).
- **Proportionality principle.** Scale of intervention (energy, area, duration) must be proportionate to expected knowledge gain and bounded by predeclared ceilings.

Bottom line. Responsible exploration of new substrates—cosmic or terrestrial—hinges on three habits: **design for reversibility**, **publish so others can falsify you**, and **build systems that default to safe, bounded behavior**. Governance is not a bolt-on; it is an architectural constraint that, when honored, makes ambitious experiments *both* safer and more scientifically credible.

12. Roadmap and Open Problems

12.1 Near-term (0–2 years): CA library, fractal P&R, small hybrid array

Objectives

- Ship an **engineerable CA stack** (rules + macrocells + simulator + compiler).
- Validate **fractal floorplanning** on multi-leaf arrays.
- Fabricate a **bench-top hybrid array** (litho anchors + rule-grown fabric) with in-situ repair.

Milestones & metrics

- **M1 — CA macrocell kit (6–9 mo).** INV, NAND2, XOR2, DFF, C-element, FIFO, router-μ; latency/area manifests; invariant checks (one token/rail/cell). *Target:* 0 functional errors over 10^9 simulated ϕ.
- **M2 — Fractal P&R (9–12 mo).** Quadtree placer, Hilbert/Peano router, H-tree clock model; timing closure with GALS shims. *Target:* 64-leaf design with ≤2ϕ skew, ≤1% routing overflows.
- **M3 — 64×64 leaf demos (12–15 mo).** RCA4, fan-out legality, 8-stage DFF pipeline, watchdog scrubbing, permanent-fault isolation. *Target:* recover transient faults in <50ϕ; contain permanent faults with ≤2× path latency.
- **M4 — Hybrid coupon (15–24 mo).** 1–4 mm^2 directed self-assembly coupon (BCP or DNA tiles) under litho ribs; post-scrub defectivity ≤10^{-7} per junction; via yield ≥99.999%; programmable crossbar or CAM slice functional with ECC.

Tooling

- Open-source **CA toolchain** (front-end synthesis → P&R → bitmap + rule table), containerized; regression farm with fault injection.
- Lab processes: solvent/thermal anneal rigs, photochemical gates, probe cards for coupon IV and sentinel readout.

Risks & mitigations

- *Routing congestion:* widen leaf channels; lower target density ρ; add second backbone lane.
- *Self-assembly drift:* denser fiducials; larger via-capture pads; increase scrub cadence.
- *Clock smear in CA sim:* add clock-repeaters; re-tile T0..T3 with phase locks.

12.2 Mid-term (2–5 years): ECC-capable self-assembly, photonic/phononic logic fabrics

Objectives

- Scale rule-driven growth to **cm-class** arrays with **on-fabric ECC**.
- Demonstrate **wave-based logic** in photonic/phononic lattices that implements dual-rail, gated collisions, and latches.

Milestones & metrics

- **M5 — ECC tiles at scale (24–36 mo).** Majority geometries + product codes on 1 cm² crossbars; automated scrub-and-heal. *Target:* post-repair bad-junction rate ≤10^{-8}; ECC overhead ≤30% area/energy.
- **M6 — Hybrid block integration (30–42 mo).** Two to three functional blocks (Crossbar-MAC + TCAM) on one die, quadtree spare map, Morton-code remap. *Target:* ≥99% tiles operational after remap; MAC error ≤1% rms.
- **M7 — Photonic/phononic logic line (36–48 mo).** Guided-mode wires, controlled-collision gates, and a phase-trap latch; 4-bit ripple carry in optics or acoustics. *Target:* BER ≤10^{-9} at kHz–MHz symbol rates; regeneration sections every 1–2 mm (optics) or 1–5 cm (acoustics).

Infrastructure

- Mask set for anchors (shuttle runs), metrology scripts for sentinel maps, thermal/optical actuation through ribs.
- Wave-lab: Kerr microresonators or waveguide arrays; phononic crystals with piezo drive; lock-in detection for sideband error channels.

Risks & mitigations

- *ECC complexity creep:* prioritize simple product / staircase codes; keep decode local and pipelined.

- *Photonic nonlinearity thresholds:* operate adiabatically; use resonant enhancement; incorporate engineered sinks to drain illegal superpositions.
- *Thermal management:* sabbath schedules; duty cycling; fractal activation patterns to spread heat.

12.3 Long-term (5–10+ years): scalable field-native emulators, targeted sky surveys

Objectives

- Build **field-native computing emulators** (BEC/optical/phononic) with parametric write/erase, fractal codes, and safety valves—running for months with low dissipation.
- Execute **pre-registered sky searches** for algorithmic structure, time-locked coincidences, and mode fingerprints.

Milestones & metrics

- **M8 — Adiabatic seeding (60–72 mo).** Parametric writing near cavity/Compton analog frequencies; $\tau_ret/\tau_write > 10^3$; deterministic erase BER $<10^{-6}$.
- **M9 — Fractal-renormalizable codes (66–84 mo).** Quadtree parity with Hilbert refresh; correct single erasures per 2×2; uncorrectable probability ~$O(p_e^2)$.
- **M10 — Year-long stability (72–96 mo).** Autonomy with watchdogs, sinks, and quench; energy/bit within 10–100× Landauer at operating T.
- **M11 — Targeted surveys (72–108 mo).** PTA/lensing/stream pipelines with preregistration, injections, and open data. *Outcomes:* either mid-compressible windows/time-locked motifs/lines at ≥5σ (multi-instrument) **or** updated exclusion regions on (coherence time, mixing, mass/self-interaction).

Ecosystem

- Community ERB for risk review; shared pipelines and simulation dictionaries; public registries of nulls and candidates.

Risks & mitigations

- *Instrument systematics mimicking structure:* multi-survey cross-checks; blinding; synthetic injections.
- *Field emulator drift:* periodic renormalization ticks; engineered sinks; automatic quench on envelope growth.

12.4 Open problems: compile-time guarantees, in-fabric learning, low-dissipation computing

Compile-time guarantees

- **Timing contracts across GALS boundaries.** Formal methods to prove L_path ≤ L_max with probabilistic wire delays and scrub pauses.
- **Deadlock-freedom for fractal NoCs.** Certificates for Hilbert/Peano backbones with credits, priorities, and detours.
- **Verification of legality masks.** Proof that local rule tables enforce global invariants (no multi-driver, no illegal merges) under all placements.

In-fabric learning

- **Learning-friendly macrocells.** On-fabric gradient/perturb-and-observe primitives compatible with dual-rail and ECC; bounded-update rules that preserve legality.
- **Plasticity vs reliability trade-offs.** Schedules that alternate compute/learn/scrub without cumulative drift; theory for stability under noisy updates.
- **Meta-compilers.** Map ML graphs to regular fabrics (crossbars, systolic arrays) with on-line calibration and fault-aware retraining.

Low-dissipation computing

- **Adiabatic pipelines.** CA and wave-fabric protocols that exploit reversible steps; quantify entropy only at sinks (errors/IO).
- **Regeneration economics.** Optimal spacing and amplitude of Rs/ticks to balance diffusion and energy.
- **Thermo-informatics.** Practical bridges from Landauer/Margolus–Levitin bounds to system-level budgets, including ECC and scrub overheads.

Hybrid manufacturing

- **Process windows with proofreaders.** Co-design chemistry and geometry to maximize energy gaps between allowed/forbidden bindings.
- **Reworkability at scale.** Localized scrub (optical/electrochemical) with guaranteed non-propagation beyond guard bands.
- **Metrology inversion.** From sentinel maps to defect causes; close the loop to process knobs automatically.

Field-native theory & observation

- **Mode dictionaries.** High-fidelity simulations that span plausible dark-sector params; priors for line ratios and Q.
- **Algorithmic null theory.** Tight bounds connecting observed compressibility to coherence and coupling in field models.
- **Ethical frameworks.** Formal “reversibility proofs” and community quench standards for any sky-facing proposal.

North star. Unify **engineering discipline** (compile, route, prove, repair) with **materials and field physics** (grow, seed, rephase, quench). The near-term delivers working CA and hybrid arrays; mid-term adds ECC and wave logic; long-term asks—and safely answers—whether nature’s quietest media can host computation, with falsifiable tests either way.

Appendices

A. Example block-CA transition tables (per primitive)

Notation (2×2 Margolus block, phase ϕ ∈ {0,1,2,3}):

- Cell states: . (void), I (insulator), C (conductor), K (corner), R (repeater), F (splitter), M (merger), V↑/V↓ (via up/down), A/B (dual-rail tokens), A^+/B^+ (overpass tokens), Tϕ (clock tile), E (error).
- A block is written row-major:
- [s00 s01
- s10 s11]
- A rule entry: (ϕ, in-pattern) → out-pattern (bijective on legal sets).
- Transport axis abbreviations: →, ←, ↑, ↓. Heading is implied by local wiring (C/K/V).

A1. Transport pass (examples)

Straight conductor (eastbound A token):

ϕ:*,

[A C

. C] → [. C

A C]

(legal only if target is empty/non-blocking conductor; else → E in logic/sanitation)

Corner turn (northbound B at K⊣):

ϕ:*,

[B K⊣

. C] → [. K⊣

B C]

Via entry/exit (plane ⇄ overpass):

ϕ:*,

[A V↑

. C] → [. V↑

A^+ C]

ϕ:*,

[A^+ V↓

. C] → [. V↓

A C]

A2. Logic/collision pass (examples)

NAND2 footprint (two orthogonal inputs meet on ϕ=2):

- Inputs: X,Y ∈ {0,1} carried as presence on A/B rails.
- Truth: Z = NOT(X AND Y) → output rail emits A if X∧Y==1, else B.

Representative rule (schematic; footprint elided):

ϕ=2:

(in_A=B=∅, in_Y=B=∅) → emit B on Z

(in_X=1, in_Y=∅) → emit B on Z

(in_X=∅, in_Y=1) → emit B on Z

(in_X=1, in_Y=1) → emit A on Z

(other overlaps) → E

("∅" = no token on that rail at the sampling cell; illegal dual-rail or mistimed arrivals → E.)

Splitter F (fan-out) discipline:

ϕ=0 check window:

if token present on input AND both outputs empty → duplicate token to both outputs at ϕ=2

else → set junction to E

Merger M (dual-rail OR) discipline:

ϕ=2:

≤1 token per rail across inputs → pass through to output

>1 token per rail → E

A3. Regeneration / sanitation

Repeater R (canonicalize 1-cell pulse; absorb smear):

ϕ=3:

any A or B spanning 1–2 cells touching R → re-emit exactly 1-cell A/B on the output port; clear neighbors

Illegal contact with Insulator I:

ϕ=3:

token adjacent to I without legal port → absorb token (.) and set E with probability 1 (deterministic)

B. Leaf-tile interface spec and latency contracts

Leaf geometry: square r×r grid (typ. 64×64 or 128×128) with standardized edge ports.

B1. Ports and signals

- **Data ports (per edge):** D[n] lanes, each lane includes:
    - A/B dual-rail token pair (data),
    - VALID side rail,
    - READY side rail.
- **Clock fabric:** contiguous T0..T3 tiling across leaf; phase continuity checkers at edges.
- **Alert/health rails:**
    - E-ALERT (slow, sticky),
    - HEARTBEAT (periodic token emission for liveness),
    - optional SCRUB-CTRL (receive scrub tokens from parent).

Electrical-style contract (token semantics):

- **VALID high** ⇒ token present on exactly one of {A,B} at the sampling site.
- **READY high** ⇒ downstream buffer available.
- Transfer occurs at **ϕ0** iff VALID∧READY. Otherwise, sender holds; back-pressure propagates.

B2. Latency/throughput budgets

- **Interface latency budget per exported net:** L_max (in ϕ steps).
    - L_path = L_leaf_out + L_interleaf + L_leaf_in ≤ L_max
    - L_interleaf = 2·H + Σ(shims) where H = backbone hops, 2 ϕ per hop.
- **Throughput per lane:** C_lane tokens per ϕ (≤ 1).
    - Burst tokens must not exceed B_max credits advertised by the adjacent router.

B3. Timing & skew tolerance

- **Intra-leaf skew:** ≤ 1ϕ (guaranteed by T-repeaters).
- **Inter-leaf skew (siblings in same quadrant):** ≤ 2ϕ.
- All cross-leaf links must pass through **GALS shims** providing two-flop (two-latch) synchronization equivalent.

B4. Health & error handling

- **E semantics:** any illegal condition at the boundary raises E-ALERT; boundary logic quarantines the port (stalls ingress), triggers local **SCRUB**, and re-opens upon **HEALTH** token acknowledging recovery.
- **Counters exposed:** per-port latency histogram, token drop count (should be zero), E-events, scrub cycles.

C. Process recipes for hybrid self-assembly (conceptual)

Intent: “anchors” by lithography; “body” by rules. Recipes below sketch controllable steps; adapt numbers to chosen materials.

C1. Directed block-copolymer (BCP) crossbar coupon

1. **Anchors (litho):** pattern graphoepitaxy trenches (depth 20–60 nm, pitch 100–200 nm) in 4×4 quadtree. Deposit/define H-tree power/clock ribs (0.5–2 µm pitch).
2. **BCP spin & anneal:** PS-b-PMMA χN≈80–120, target period 12–20 nm. Spin at 2000–4000 rpm; solvent vapor anneal (THF or toluene) 10–30 min.
3. **Selective removal:** UV/ozone or acetic acid to remove PMMA; verify domain order via SEM/sentinel dye.

4. **First metal fill:** electroless Cu/Co plating into pores (word lines). Rinse, dry; ALD Al_2O_3 (2–5 nm) as spacer.
5. **Orthogonal pass:** rotate by 90°, repeat BCP steps for bit lines (using orthogonal trenches).
6. **Proofread scrub:** gentle solvent/thermal pulse; sentinel readout; repeat once if defectivity > threshold.
7. **Via capture:** self-aligned via etch landing on oversized pads connected to H-tree ribs.
8. **Passivation:** polymer cap; optional CMP for planarity.

Targets: post-scrub defectivity ≤ 10^{-7}/junction; via yield ≥ 99.999%.

C2. DNA tile CAM slice (30 nm pitch)

1. **Anchors:** fiducials & I/O islands; gold pads (functionalizable) arranged in Morton-code grid.
2. **Tile assembly:** fold 30–40 nm origami rectangles with addressable toeholds {τ0,τ1,τ2}; attach Pd/Au seeds at vertices.
3. **Directed placement:** flow tiles; electrostatic guide via biased ribs; incubate 10–60 min.
4. **Kinetic proofreading:** fuel strand cycles to eject mis-bound tiles; optical activation stripe-by-stripe.
5. **Metallization:** electroless growth at seeds, forming conductive islands/links; ALD dielectric spacing.
6. **Majority voters:** geometric Y-merges every N cells; sinks for disagreeing triplets.
7. **Scrub & lock:** final displacement to passivate toeholds; seal with thin oxide.

Targets: majority correction ≥ 99.99%; match-line continuity ≥ 99.999% after remap.

C3. Photonic/phononic crystal band-gap tile

1. **Anchors:** pattern coupling gratings and H-tree heaters/actuators.
2. **Self-assembly:** colloidal spheres (photonic) or block-copolymer hard mask (phononic) to form periodic lattice.
3. **Infiltration:** high-index (TiO_2) or high-stiffness (Si_3N_4) via ALD/SIS.
4. **Defect writing:** local heat/UV to tune defect cavities (phase traps).

5. **Characterization:** measure bandgaps/Q via out-couplers; map with sentinel sidebands.

Targets: bandgap uniformity within 5%; Q within 10% of design across cm scale.

D. Glossary of terms and symbols

- **A/B (dual-rail tokens):** Presence-encoded logic rails; A carries logical 0 on rail-0, B carries logical 1 on rail-1. Illegal = both/none at sample time.
- **A^+/B^+ (overpass tokens):** Dual-rail tokens on a non-interacting "over" layer, accessible via V↑/V↓.
- **Adiabatic (drive):** Parameter change slow enough to avoid exciting unwanted modes; used for low-dissipation write/regenerate steps.
- **Alert rail (E-ALERT):** Slow channel that carries sticky error notifications to supervisors.
- **Backbone (Hilbert/Peano):** Space-filling global interconnect preserving locality; provides predictable latency and routing.
- **BCP (block-copolymer):** Phase-separating polymer used for self-assembled masks/structures.
- **C-element (Muller):** Gate that outputs a value only when all inputs agree; used for joins/synchronization.
- **CA (cellular automaton):** Discrete lattice with local update rule; here, engineered for wires/gates/clock.
- **Chiplet:** Cluster of leaves acting as a module with internal high-rate clocking.
- **ECC (error-correcting code):** Redundancy to detect/correct defects; e.g., product or staircase codes.
- **E (error state):** Sticky local state indicating rule violation; opaque to normal transport; triggers scrub/containment.
- **F/M (splitter/merger):** Macrocells that fan-out and fan-in tokens under legality guards.
- **GALS:** Globally Asynchronous, Locally Synchronous; phase-managed islands with handshake crossings.
- **H-tree (clock/power):** Fractal tree with equal path lengths to leaves, minimizing skew/IR drop.

- **K (corner):** Conductor with a 90° turn; orientation implied by local geometry.
- **Latency L_path:** End-to-end ϕ-steps from source to sink, including gates, wires, and hops.
- **Leaf (tile):** Small, regular CA region (e.g., 64×64) with standardized boundary ports.
- **Margolus (partition):** 2×2 block update scheme alternating offsets; ensures conflict-free permutations.
- **MVIS:** Minimum Viable Intelligent Substrate—statefulness, controllability, transport, error economics.
- **NoC (network-on-chip):** Here, the fractal backbone + routers linking leaves/chiplets.
- **Overpass (via):** Temporary lift of tokens to a non-interacting layer to cross without collision.
- **Parity/majority tiles:** Local ECC geometries that vote or compute parity over groups.
- **READY/VALID:** Flow-control rails implementing back-pressure and lossless transfer.
- **Repeater (R):** Canonicalizes pulse shape/phase; placed periodically along wires.
- **Sanitation:** Rule stage that absorbs illegals, resets shapes, and prevents contamination propagation.
- **Scrub:** Scheduled repair pass (in CA or materials) that resets/cleans erroneous regions.
- **Sierpinski guard:** Fractal containment perimeter that stops defect propagation and defines isolation cuts.
- **Tϕ (clock tile):** Local state carrying clock phase; advances modulo-4; governs rule sub-stages.
- **TMR (triple modular redundancy):** Triplicate logic with majority voting for single-fault tolerance.
- **Via V↑/V↓:** Entry/exit states for the overpass layer; legalize crossings.
- **WOF (wiring overhead factor):** Multiplier capturing extra cells/area from routing and repeaters beyond logic macrocells.

Usage note: These appendices are meant as implementation scaffolding. A working prototype can start with the A-section rule snippets, adhere to the B-section interface/latency contracts,

follow the C-section recipes for first coupons, and lean on the D-section glossary to keep nomenclature consistent across teams and toolchains.

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Notes:

• Citations emphasize foundational texts and broad reviews to keep the bibliography stable and accessible; more specialized or recent results can be added in a longer version.

• Entries connect directly to the paper’s pillars: engineerable CA and fractal P&R ([3],[8]–[13]), hybrid self-assembly and ECC ([16]–[22],[46]–[47]), wave/field computing and dark-sector candidates ([24]–[31]), and observational/algorithmic tests with thermodynamic bounds ([32]–[41]).